UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/615,837 | 07/13/2000 | Toshihiro Shigemori | R2184.0080/P080 | 6793 |

24998 7590 07/08/2004

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

| EXAMINER | |
|---|---|
| BATTAGLIA, MICHAEL V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2652 | |

DATE MAILED: 07/08/2004

10

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/615,837 | Applicant(s) SHIGEMORI, TOSHIHIRO | |
|---|---|---|---|
| | Examiner Michael V Battaglia | Art Unit 2652 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,5 and 6* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This action, dated June 30, 2004, is in response to Applicant's amendment, filed May 28, 2004 and entered as a result of the RCE filed on June 17, 2004. Claims 1-6 are pending.

### *Claim Objections*

1. Claim 4 is objected to because of the following informality. On line 6 of claim 4, replacing "dick" with -disk— is suggested. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al (hereafter Saito) (US 5,377,178).

Saito discloses a data recording clock signal generator (Col. 28, lines 23-61) that generates a recording clock signal synchronous with a wobble signal used for recording data on an optical disk having a data recording track wobbled by the wobble signal having predetermined frequency components (Col. 3, lines 40-46 and Col. 5, lines 35-43), said data recording clock generator comprising: a wobble signal extracting unit that extracts the wobble signal (Fig. 3 and Fig. 15, element 606); a recording clock signal dividing unit that generates a divided clock signal obtained by dividing the frequency of the recording clock signal (Fig. 24, element 1210); a phase difference signal generating unit that generates a phase difference signal as a result of phase comparison

between the wobble signal and the divided clock signal (Fig. 24, element 1200); a frequency control signal generating unit that generates a frequency control signal based on the phase difference signal generated by the phase difference signal generating unit (Fig. 24, elements 1202 and 1204); and a recording clock signal generating unit that generates the recording clock signal having a frequency controlled in accordance with the frequency control signal generated by the frequency control signal generator (Fig. 15, element 610 and Fig. 24, element inside the dashed lines), wherein the recording clock signal dividing unit is provided with a frequency dividing rate setting unit that sets a reference frequency dividing rate by which the frequency of the recording clock signal is divided and a frequency dividing rate different from the reference frequency dividing rate, following predetermined procedures (Fig. 24, elements 1212 and 1214), and wherein a phase relationship between the wobble signal and the recording clock signal can be changed by a unit smaller than one clock cycle of the recording clock signal each time the frequency dividing rate setting unit changes its setting (Col. 19, lines 47-52 and Col. 28, lines 53-56). The examiner interprets the initial frequency dividing rate as the reference frequency dividing rate and the frequency dividing rates different from the initial frequency dividing rate as being frequency dividing rates different from the reference frequency dividing rate. The examiner notes that the PLL circuit inside the dashed lines of Fig. 24 inherently has an initial frequency dividing rate because an initial frequency dividing rate is needed for the PLL to be a stable oscillating source. Further the PLL is an analog circuit that adjusts phase relationship by an amount needed to align the phases of the signals. The adjustment unit is as small or large as misalignment between the phase of the signals and certainly includes an adjustment unit smaller than one clock cycle of the recording clock signal. The phase relationship between the wobble signal and the recording clock signal is adjusted or changed any time the phases of the signals are unaligned, which includes each time the frequency dividing rate

setting unit changes its setting. Therefore, the phase relationship can be changed each time the frequency dividing rate setting unit changes its setting or any other time the phases of the signals may become unaligned.

***Allowable Subject Matter***

3. Claims 2, 3, 5 and 6 are allowable over the prior art of record.

4. Claim 4 would be allowable if rewritten or amended to overcome the objection set forth in this Office action. None of the references of record alone or in combination disclose or suggest a data recording clock signal generator that generates a recording clock signal synchronous with a wobble signal used for recording data on an optical disk having a data recording track wobbled by the wobble signal, which has predetermined frequency components, and on which address information and a synchronizing signal are phase-modulated and superimposed, a groove of the data recording track being formed on the optical disk in a phase-modulated manner, said data recording clock signal generator comprises: a wobble signal extracting unit that extracts the wobble signal; a recording clock signal dividing unit that generates a divided clock signal obtained by dividing a frequency of the recording clock signal; a phase difference signal generating unit that generates a phase difference signal as a result of a phase comparison between the wobble signal and the divided clock signal; a frequency control signal generating unit that generates a frequency control signal based on the phase difference signal generated by the phase difference signal generating unit; a recording clock signal generating unit that generates the recording clock signal having a frequency controlled in accordance with the frequency control signal generated by the frequency control signal generating unit; and a masking unit that generates a phase comparison mask signal to prevent the phase difference signal generating unit from generating the phase

difference signal, **said mask signal being generated at a portion of the wobble signal on which either the address information or the synchronizing signal is phase modulated and superimposed on the optical disk.**

### *Response to Arguments*

5. Applicant's arguments filed March 28, 2004 with respect to claim 1 have been fully considered but they are not persuasive. It is noted that Applicant is only claiming that the phase relationship **can** be changed each time the frequency dividing rate setting unit changes its setting. As described above, the phase relationship can be changed each time the frequency dividing rate setting unit changes its setting because the phase relationship is changed any time the phases of the signals are unaligned, which includes each time the frequency dividing rate setting unit changes its setting. As described above and in the Office action dated March 18, 2004, the PLL of Fig. 24 is an analog circuit and the adjustment unit of the phase relationship change is as small or large as misalignment between the phase of the signals, which would certainly include an adjustment unit smaller than one clock cycle of the recording clock signal.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Battaglia

HOA T. NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600
7/2/04